CLAIMS

1. (previously presented) A method of providing first and second output signals in response to first and second input signals during first and second clock states, comprising:

providing the first and second input signals at logic states that are complementary during the first clock state;

providing first and second intermediate signals on first and second nodes at logic states that are complementary in response to the step of providing the first and second input signals;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing both the first and second input signals at a predetermined one of the complementary logic states during the second clock state;

enabling the clock inputs of the first and second clocked inverters in response to a transition from the first clock state to the second clock state whereby the first and second intermediate signals at the complementary logic states are latched; and

providing the first and second output signals responsive to the first and second intermediate signals.

2. (withdrawn) The method of claim 1, wherein the first and second clocked inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

3. (canceled).

4. (original) The method of claim 1, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

5. (canceled)

6. (original) A method of providing first and second output signals in response to first and second input signals, comprising:

providing the first and second input signals at complementary logic states;

providing first and second intermediate signals on first and second nodes at the complementary logics states in response to the providing the first and second input signals at the complementary logic states;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing the first and second input signals at a predetermined one of the complementary logic states during a precharge phase;

enabling the clock inputs of the first and second clocked inverters in response to entering the precharge phase; and

providing the first and second output signals responsive to the first and second intermediate signals.

7. (withdrawn) The method of claim 6, wherein the first and second inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

8. (original) The method of claim 6, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

9. (original) The method of claim 8, wherein the third and fourth clocked inverters are characterized as inverting only one of the complementary logic states when the clock inputs are disabled and inverting both logic states when the clock inputs are enabled.

10. (previously presented) A circuit, comprising:

a first clocked inverter having a signal input for receiving a first input signal and an output, wherein the first clocked inverter is enabled during a first clock state;

a second clocked inverter having a signal input for receiving a second input signal complementary to the first input signal during the first clock state and an output, wherein the second clocked inverter is enabled during a the first clock state and the first and second input signals are in a same logic state during a second clock state;

a third clocked inverter having a signal input coupled to the output of the first clocked inverter and an output, wherein the third clocked inverter is enabled during the second clock state;

a fourth clocked inverter having a signal input coupled to the output of the second clocked inverter and an output, wherein:

the fourth clocked inverter is enabled during the second clock state; and

the output of the fourth clocked inverter is coupled to the input of the third clocked inverter and the output of the third clocked inverter is coupled to the input of the fourth clocked inverter.

11. (original) The circuit of claim 10 further comprising:

a first inverter having an input coupled to the output of the first clocked inverter and an output for providing a first output signal; and

a second inverter having an input coupled to the output of the second clocked inverter and an output for providing a second output signal.

12. (previously presented) The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to a first power supply terminal, and a second current electrode;

a second transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for receiving the clock signal, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

13. (previously presented) The circuit of claim 12, wherein the third clocked inverter comprises:

a fourth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second power supply terminal, and a second current electrode coupled to the output of the second clocked inverter;

a fifth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second current electrode of the fourth transistor, and a second current electrode; and

a sixth transistor having a control electrode for receiving the clock signal, a first current electrode coupled to the second current electrode of the fifth transistor, and a second current electrode coupled to the first power supply terminal.

14. (original) The circuit of claim 13, wherein the third and fourth transistors are P channel transistors.

15. (previously presented) The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control input for receiving the first signal, a first current electrode coupled to a first power supply terminal, and a second current electrode coupled to the signal input of the third clocked inverter;

a second transistor having a control input for receiving the clock signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for being enabled during the first clock state, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

16-26. (canceled)